DISTRIBUTED PACKET PROCESSING ARCHITECTURE FOR ACCESS SERVERS

ABSTRACT OF THE DISCLOSURE

An access server architecture, and methods for use of the architecture, are disclosed. The architecture and methods are designed to increase the scalability of and balance processor load for a network access server device. In this architecture, packet forwarding and packet processing are distributed amongst the cards serving the low-speed access lines (i.e., line cards), such that each line card is responsible for performing forwarding and packet processing for packets associated with the low-speed ports that line card serves. Thus, as the number of line cards expands, forwarding resources are expanded in at least rough proportion.

The NAS route switch controller, as well as the high-speed ports used to access the network, are largely relieved of packet processing tasks for traffic passing through the server. The egress port uses a distribution engine that performs a cursory examination on one or more header fields on packets received at the high-speed interface—comprehending only enough information to allow each packet to be distributed to the appropriate line card for full packet processing. The route switch controller updates the routing information needed by each distribution or forwarding engine, and is largely uninvolved in the processing of individual packets.